CBCS SCHEME

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18EC34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Design a combinational circuit to output the 2's complement of a 4-bit binary number. **(07 Marks)**

b. Identify all prime implicants and essential prime implicants of following function using K-map:
$f(a, b, c, d) = \sum m + (6, 7, 9, 10, 13) + dc(1, 4, 5, 11, 15)$. Draw the diagram using NAND gates. **(07 Marks)**

c. Expand the following in to canonical form and represent in decimal form:
i) $f_1 = a + bc + ac'd$ in to min-terms
ii) $f_2 = a(b + c)(a + c + d)$ into max terms. **(06 Marks)**

OR

2 a. Find the minimal sum of the following Boolean function using Quine-McClusky method:
$f(a, b, c, d) = \sum m (7, 9, 12, 13, 14, 15) + dc (4, 11)$. **(07 Marks)**

b. Using K-map determine minimal product of sum expressions an implement the simplified equation using only NOR gates:
$f(w, x, y, z) = \pi(1, 2, 3, 4, 9, 10) + d(0, 14, 15)$. **(07 Marks)**

c. Explain briefly K-map, Incompletely specified functions, essential prime implicants and Gray code. **(06 Marks)**

Module-2

3 a. Implement the following using 3 to 8 decoder with active low enable and active HIGH outputs:
i) $f_1(a, b, c, d) = \sum m (0, 1, 5, 6, 7, 9, 10, 15)$
ii) $f_2(a, b, c) = \pi(1, 3, 6, 7)$ **(06 Marks)**

b. Explain 4-bit carry look-ahead adder with necessary diagram and relevant expressions. **(08 Marks)**

c. Design 4 line to 2 line priority encoder which gives MSB the highest priority and LSB least priority. **(06 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \sum(0, 4, 8, 10, 14, 15)$ using
i) 8:1 MUX with a, b, c as select lines
ii) 4:1 MUX with a, b as select lines. **(06 Marks)**

b. Design a two bit magnitude comparator and draw the neat diagram. **(08 Marks)**

c. Explain the structure of programmable logic arrays (PLA) with an example. **(06 Marks)**

Module-3

5 a. Explain clocked SR flip flop using NAND gates with necessary truth table and waveform. **(06 Marks)**

b. Explain with a neat diagram and truth table, a 4-bit SIPO shift register to store binary number 1011. **(07 Marks)**

c. What is race around condition? Explain JK master slave flip flop with a diagram, function table and timing diagram. **(07 Marks)**

OR

6 a. Explain with an excitation table, the conversion of SR flip flop in to JK and D flip flop. **(06 Marks)**

b. Explain the working of 4-bit Twisted Ring counter using necessary diagram and waveform. **(07 Marks)**

c. Explain the working of 3-bit Asynchronous up-down counter with necessary waveform and truth table. **(07 Marks)**

Module-4

7 a. Design a self correcting synchronous counter using positive edge triggered JK flip flop to count 0, 1, 2, 4, 5, 6, 0, 1, 2…. Use the state table and state diagram. **(10 Marks)**

b. Design a clocked sequential circuit which operates according to the state diagram shown in Fig.Q.7(b). Implement the circuit using negative edge triggered JK flip-flop. **(10 Marks)**

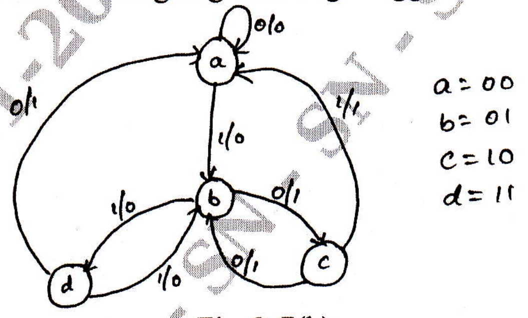

Fig.Q.7(b)

OR

8 a. Construct the excitation table, transition table, state table and state diagram for the sequential circuit shown in Fig.Q.8(a). **(10 Marks)**

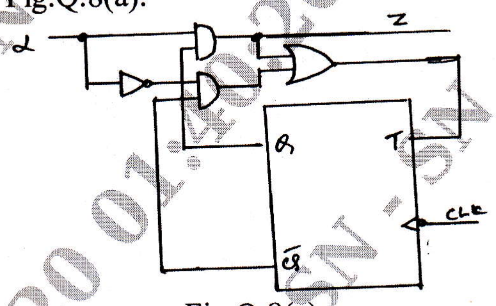

Fig.Q.8(a)

b. Realize synchronous decade counter using T-flip-flop and draw the neat diagram. **(10 Marks)**

Module-5

9 a. Design a Melay type sequence detector to detect the sequence of 101 in the given sequence of 001101100101011. **(10 Marks)**

b. With necessary diagram, explain the concept of serial adder with accumulators. **(10 Marks)**

OR

10 a. Design a sequential circuit to convert BCD to Excess-3 code with state table, state graph and transition table. **(10 Marks)**

b. Explain the design of sequential circuit using CPLDs and give CPLD implementation of a shift register and parallel adder with accumulator. **(10 Marks)**

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